# ELECTRONIC DEVICES BASED ON SEMICONDUCTING TRANSITION METAL DICHALCOGENIDES

BY

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THESIS

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## Abstract

Semiconducting transition metal dichalcogenides (TMDs) possess great potential as the channel material for next-generation electronic and optoelectronic devices due to their atomically thin body without surface dangling bonds and tunable bandgaps. This thesis investigates various transistors based on exfoliated and synthesized TMD materials. As a base for the results reported in this thesis, the fabrication processes are developed with key steps and parameters presented in detail. The characterization methods are established and elaborated, including the home-built photocurrent measurement setup and Labview programs.

The electrical properties of CVD synthesized monolayer $MoS_2$ and $WSe_2$ are investigated. The mobilities are extracted from back gate transistors, where the contact resistance is excluded with 4-point measurement for $MoS_2$, and the histogram of mobilities is summarized for $WSe_2$.

Three different device structures based on exfoliated few-layer $MoTe_2$ are proposed and fabricated: back gate transistor, suspended transistor, and double gate transistor. The contrast-thickness correlation and Raman spectra of few-layer $MoTe_2$ are obtained. Room-temperature ohmic contact and low electron barrier are found for Cr contacted $MoTe_2$. Schottky barrier limited behavior is revealed through variable temperature measurement. The mobility of a 10 nm thick $MoTe_2$ reaches 8 $cm^2/V{\cdot}s$. The bandgap of $MoTe_2$ is extracted using optical and electrical methods with consistency. The intrinsic mobility of $MoTe_2$ is revealed by suspended transistors. Room temperature mobility at 108 $cm^2/V{\cdot}s$ is recorded, which is twice as large as the supported device due to reduced phonon scattering. The low-temperature mobility is found limited by charged impurities, which diverges significantly from supported devices due to the absence of dielectric screenings. In addition, Raman spectroscopy shows enhanced out-of-plane vibration in the suspended channel. Additional control of the doping density and vertical electric field is introduced in double gate transistors. Polarity switching and polarity pinning in double-gated devices are understood by separating the electrostatic effect on contact and channel. The intrinsic conductance under the vertical electric field is studied, and the photocurrent mechanism is presented.

# Acknowledgments

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# Contents

# 1. Introduction

Transition metal dichalcogenides (TMDs) are a group of layered materials with three layers of covalently-bonded atoms in each layer, where one layer of transition metal is sandwiched in between two layers of chalcogenide group elements. The general composition of TMDs can be expressed as $MX_2$, where M represents one transition metal such as Mo, W, and X represents chalcogenide atoms chosen from S, Se, and Te. Mo and W based TMDs are semiconductors in the 2H phase [1-4]. Monolayer Mo and W baed TMDs show direct bandgaps with great potential as optoelectronic devices. As the chalcogenide atom evolves from S to Se and Te, the bandgap of semiconducting 2H Mo-based TMDs decreases from 1.8 eV in monolayer $MoS_2$ to 1.2eV in monolayer $MoTe_2$ [4-6]. They also exhibit the same trends in the thickness evolution of bandgaps, where the bandgap decreases as thicknesses increases, and undergo direct-indirect transition at two layers [5]. Compared with $MoS_2$ and $WSe_2$, $MoTe_2$'s photoresponse lies in the infrared region with a small bandgap between 1.0eV and 1.2eV depending on the thickness, which is similar to Si. These optical bandgaps extracted for monolayer are lower than electrical bandgap due to large exciton binding energies [6, 7]. The electrical bandgap refers to the energy gap between the conduction band minimum and the valance band maximum. The extraction of the electrical bandgap is reported for black phosphorus (BP) and $WSe_2$ through the Schottky barriers for different carriers [8, 9]. The bandgap of BP can also be extracted through temperature-dependent minimum conductance [10]. The bandgap tuning is reported for graphene, BP, and $MoS_2$, where the bandgap will decreases when a vertical electric field is applied [10-12]. As a fundamental physical parameter, accurate electrical bandgaps are essential to the modeling and design of devices.

Semiconducting TMDs are also appealing for logic devices. The mobility of conventional 3D semiconductors is hindered by the surface scattering in the thin channel, while layered semiconductors have an atomically flat surface which is free of dangling bonds. Moreover, the ultra-thin body also demonstrates a high resistance to short channel effect, which is ideal for future technology node with extreme scaling [3, 13]. High electron mobility and hole mobility are reported for monolayer $MoS_2$ and $WSe_2$ respectively [14, 15]. The room temperature mobility of $MoS_2$ is mainly limited by the polar optical phonon [16, 17]. BN encapsulation eliminates interface traps from dielectrics and improves the room temperature mobility of $MoS_2$ [18]. The interface trap also contributes to the degradation in the subthreshold swing. High-k dielectric materials can improve the mobility due to enhanced dielectric screening. However, the additional remote phonon scattering also limits the mobility [15, 19, 20]. CVD

synthesized materials typically have smaller mobility due to the high defect density and grain boundary [21]. To avoid the interface trap and phonon scattering from the substrate, suspended transistors with vacuum as the dielectric are reported. High channel mobility and low subthreshold swing due to the absence of interface trap and optical phonon scattering are presented in a suspended $MoS_2$ channel [22, 23]. The suspended transistor provides an ideal platform to investigate the intrinsic transport behavior of 2D semiconductors. Compared with $MoS_2$ and $WSe_2$, $MoTe_2$ has weak Fermi level pinning and high phonon limited mobility [24-27]. These favorable properties of $MoTe_2$ make it highly suitable for logic applications.

Another obstacle for 2D semiconductors is the difficulty in achieving nmos and pmos with the same material due to the difficulty in doping. This difficulty is also a major cause of large Schottky barriers between metal-2D semiconductor contacts. Improving channel conductivity and reducing contact resistance are essential for high on-current transistors. Proximate chemical doping from small molecules and non-stochastic oxide is exploited to reduce the Schottky barrier height and contact resistance [28-30]. Aside from chemical doping, electrostatic doping is more flexible for reconfigurable devices. By doping the semiconductors into heavily doped n-type or p-type, a Schottky barrier that is thin enough allows tunneling injection into semiconductors, which reduces contact resistance. In addition, the dynamic control of n and p-type allows polarity switching [31, 32]. The switching between tunneling FET and MOSFET is also achieved through electrostatic doping [33]. Moreover, ferroelectric dielectrics enable non-volatile electrostatic doping which can be used for memory and reconfigurable logic applications [34-36]. Among TMDs materials, the polarity of $MoTe_2$ is conveniently controlled due to a small bandgap and weak Fermi level pinning, which opens vast opportunities for reconfigurable devices.

# 2. Fabrication and characterization methods

## 2.1 Exfoliating and stacking 2D materials

The typical methods to get thin 2D flakes are exfoliation and direct synthesis. $MoS_2$ and $WSe_2$ devices are fabricated based on monolayer synthesized by chemical vapor deposition (CVD). Due to the air sensitivity of thin layer $MoTe_2$, the $MoTe_2$ flakes are exfoliated right before fabrication. The wide-adopted exfoliation procedures are described in [37]. Before the exfoliation, 15 cm of Scotch tape is cut and a piece of $MoTe_2$ bulk material is carefully placed on it. Then, the tape is folded and separated several times to spread $MoTe_2$ over the whole tape. The exfoliation starts by cleaning Si substrates with 90nm $SiO_2$ in piranha solutions for 10 minutes, followed by 6 minutes of oxygen plasma cleaning. The prepared tape is pressed onto cleaned substrates. The stack of tape and substrate is subsequently heated on a 100° C hot plate for 2 minutes. After cooling down to room temperature, the tape is peeled off, and the substrate is examined under the microscope for thin flakes. The typical image for thin $MoTe_2$ thin flakes is shown in Figure 1(a). The thicknesses of the flakes are confirmed by atomic force microscopy (AFM). Then, the contrasts between the flake and the substrate for different layer thicknesses are measured and presented in Figure 1(b). The images used for contrast measurements are taken with identical exposure settings. The contrast starts from -45% for monolayer $MoTe_2$ and decreases to <-60% for bilayer and trilayer. It then increases starting from the quad-layer, and the intensity of $MoTe_2$ flake is stronger than the background substrate at 9 layers. Note that $MoTe_2$ flakes with the same thicknesses will show different contrasts on Si substrate with 90nm $SiO_2$ and 280nm $SiO_2$.

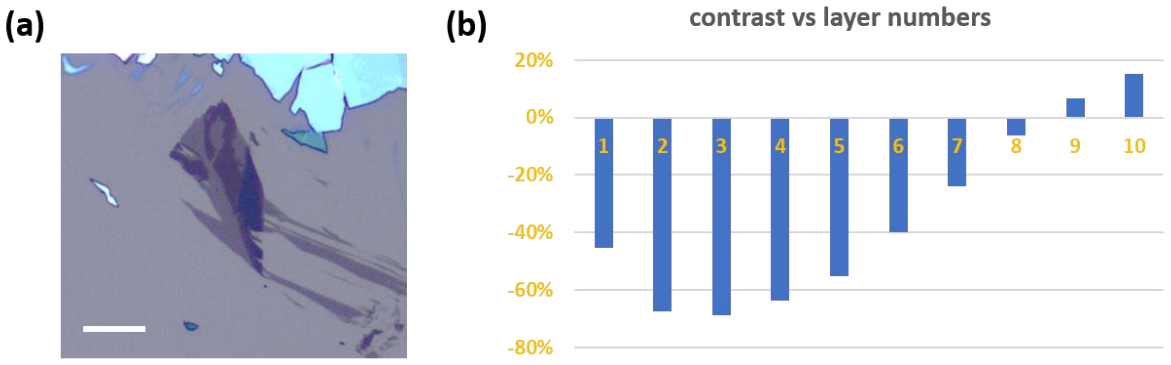


Figure 1. (a) Typical images of thin $MoTe_2$ flakes. The scale bar is 20μm. (b) The optical contrast versus layer number of $MoTe_2$ on Si substrate with 90nm $SiO_2$.

A more flexible alternative method is to use a PDMS stamp as the transfer substrate [38, 39]. The setup used for transferring flakes is shown in Figure 2(a), and the reference procedure is described in Figure 2(b). A piece of PDMS stamp (gel film) is first pressed on the prepared tape. After peeling off, the stamp is attached on a glass slide and examined under the microscope. If the desired flake is found, the stamp is cut and only keeps a small region that contains the desired flake. Then, the flake is transferred onto a Si substrate with $SiO_2$ through press-and-release. Due to the strong van der Waals force between $MoTe_2$ and $SiO_2$, the flake is separated from the PDMS stamp in the release step. This procedure allows multiple devices on the same substrate while controlling the device positions. It also allows stacking different materials to form heterostructures such as BN/$MoTe_2$ stacks.

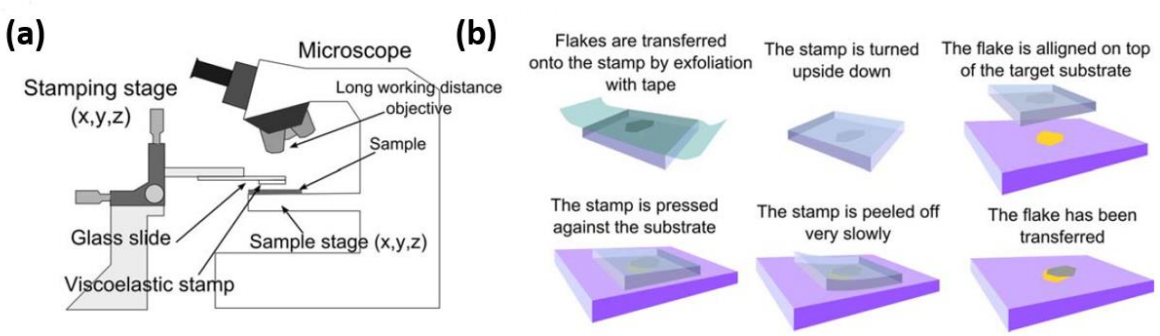


Figure 2. (a) Setup of the transfer stage. (b) Steps of the transfer process. The flake is first transferred to the stamp from the prepared tape and then transferred to the substrate under the microscope with the assist of glass slides. Reprinted with permission from [38].

When fabricating the top gate with hBN as the top dielectric, a pick-up method detailed in [40] can provide higher productivity. The procedure is described in Figure 3. The stamp used here is a bilayer of PDMS and PPC. The viscosity of the PPC layer can be controlled through temperature. At 40°C, it possesses high adhesion and it can pick up hBN or hBN/$MoTe_2$ stack from $SiO_2$ surface. At 110°C, the PPC layer is softer and less sticky so that the stacks sticks to the $SiO_2$ surface. The hBN is essential in this process since it poses good adhesion to $MoTe_2$. The hBN flake can also be used to pick up graphene, $MoS_2$ and $WSe_2$. However, it was not able to pick up $TiSe_2$ flake from $SiO_2$, which is presumably due to the weak adhesion force between hBN and $TiSe_2$. Although the pick-up method is natively suitable for the top-down process, it also allows the vertical flipping of the 2D stacks by transferring on a clean PDMS stamp, where more layers can continue to stack on both sides. Since both PDMS stamps and PPC layers used here may introduce organic contamination, thorough cleaning is required after each transfer

process. The substrates with transferred flakes are soaked in acetone for 10 minutes and dried with $N_2$ after rinsing with IPA. Since the transferred flakes are not covalently bonded to the substrates, gentle movement is preferred to avoid washing off the flakes.

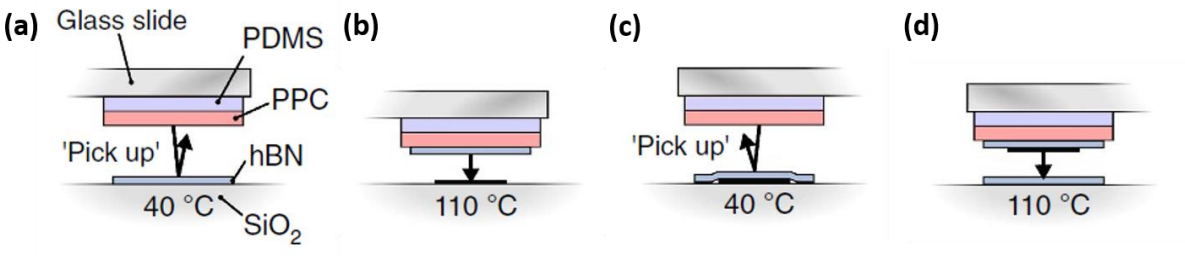


Figure 3. The procedure of fabricating the hBN/graphene stack using the pick-up method. Different temperatures are used to control whether to pick-up or drop-down through different adhesion forces of PPC. Reprinted with permission from [40].

## 2.2 Device fabrication processes

The fabrication process of back gate transistors includes lithography I, alignment mark deposition, lithography II, etching, lithography III, and metal contacts deposition. Spin coating of photoresist and developing are done before and after each lithography respectively, and metals are lifted off after each deposition. Both photolithography and e-beam lithography are used. Photolithography has been used widely in both industry and laboratory research, and it is highly suitable for back-gated transistors. However, photolithography has several shortcomings. First, the sizes of CVD samples are a few tens of micrometers and the resolution of photolithography limits the density of printable patterns. Besides, the position and morphology of CVD flakes are unpredictable and each device needs individual photolithography. Moreover, the exposure to the alkaline ions and photoresist residue may lead to unintentional doping and degradation of channel mobility. Hence, e-beam lithography is preferable due to its highly customized patterns, minimal ion exposure, and less residue. For the devices presented in this thesis, except for the CVD samples, all have been fabricated with both photolithography and e-beam lithography.

The photolithography is done with Karl Suss MJB-3 aligner with a 365nm wavelength. Photoresist AZ5214 is used and the developing process is done in AZ400K developer. The e-beam lithography is performed on a Raith e-line system. The silicon substrate with either CVD-synthesized or exfoliated flakes is first coated with a thin PMMA layer. The PMMA used for the fabrication is PMMA 495K A4,

which compromises the resolution and photoresist residue. The spinning setup is 1500-3000rpm for 30s. A small spinning rate is used for transferred thin flakes to avoid the formation of wrinkles. The accelerating voltage is set as 10kV. The substrate is developed in IPA: MIBK 3: 1 solution for 30s. To minimize residue and compensate for the current fluctuation as well as accommodating different PMMA thicknesses, the exposure dose is set to a high value of 130μC/cm$^2$.

The alignment and stitching are essential for reliable pattern transfer in e-beam lithography. In the Raith e-line, the stage position measured by the laser interferometer is the most accurate reference. During the alignment process, the coordinate of the sample under lithography is extracted based on three points with known coordinates, so that the pattern from the design file can be projected according to the sample coordinate. The extracted sample coordinate contains three sets of parameters, zoom, shift, and rotate. The effects of these parameters are illustrated in Figure 4(a). Stitching error occurs when the zoom and rotation parameters are not aligned precisely. The patterns in Figure 4(b) are alignment marks typically used. The corner of squares and the center of crosses are used as reference points under scanning electron microscopy (SEM).

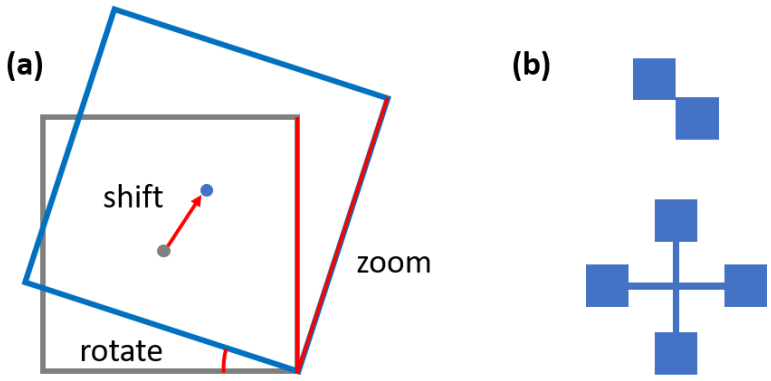


Figure 4. (a) Illustration of parameters of sample coordinate. (b) The fine patterns used as reference points in alignment.

The time expenditure is also of great importance in e-beam lithography. Large features such as electrode pads can take a few hours of exposure. The parameters of concern here are the aperture size, step size, and writing field size. For small and large features with different resolution requirements, different parameter sets are adopted. First, the writing field size is selected as 200μm for large features and 100μm for small features. Larger writing field size up to 400μm can be used given the alignment accuracy is satisfied. The aperture size used is 120μm to allow higher current for large features, while the regular features use 30μm. Large step size is needed for large writing field size to keep the beam speed below 10mm/sec, and the dose factor also needs to increase accordingly to improve the

uniformity. Figure 5(a) shows that without increasing the dose factor, the residue of PMMA causes a rough surface of the metal pad. Correction to the aperture and stigmatism as well as sample coordinate alignment is needed for each aperture size. These procedures allow patterning $mm^2$ features.

Among the three lithography steps, the first lithography step is only necessary for e-beam lithography to transfer the alignment marks on the substrate for subsequent lithography. 5nm Ti/ 20nm Au is used in metal deposition, where Ti acts as an adhesion layer. An alternative method is to etch $SiO_2$ off from the exposed surface and remove the PMMA afterward. This process works for silicon substrates with $SiO_2$ less than 90nm thick. The second lithography defines the shape of TMD flakes, which affects the behavior of fabricated devices in several ways. First, the source and drain may have different contact resistances due to different widths. Moreover, the nearby metal pads might alter the current path, which often appears as an offset voltage in the hall-bar structure. Shaping the flakes into regular patterns can avoid such factors. PlasmaThermo 790 Reactive Ion Etching(RIE) is used to etch off TMD materials. Fluorine-contained gases are effective in etching TMD materials due to the volatility of reaction products as compared to $O_2$. The gases used for etching are 15sccm $CF_4$. After 30s etching, an additional 30s etching with 15sccm $O_2$ is needed to remove the carbon-fluorine layer on the surface of PMMA. Figure 5(b) shows the carbon-fluorine layer without the second $O_2$ cleaning. Then the PMMA layer is rinsed out with acetone. The third lithography defines the metal electrodes. Although adhesion layers are used for devices, strong agitation may peel off the metal on 2D flakes due to the weak bonding between synthesized materials and the substrate, especially in water or organic solvent [41]. Figure 5(c) shows a flake exposed to water with part of itself washed away. It is best to slowly shake the container and use pipette gently to remove excess metal. Using Cr as the adhesion layer can mitigate the problem since the Cr layer is rigid enough to endure agitation.

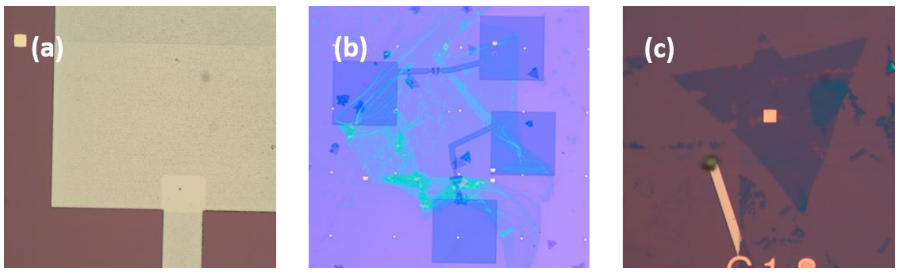


Figure 5. Typical pitfalls in lithography processes. (a) The residue of PMMA due to insufficient dose for large write field size. (b) The carbon-fluorine layer introduced by RIE on the substrate surface. (c) A partially destructed flake due to exposure to water.

Back-gate transistors with CVD synthesized $MoS_2$ and $WSe_2$ are fabricated with e-beam lithography. Both photolithography and e-beam lithography are adopted for $MoTe_2$ back gate and double gate devices. In the fabrication of back gate $MoTe_2$ transistors, the $MoTe_2$ is first transferred to the silicon substrate with oxide. For photolithography devices, only the third lithography step is needed, while both the first and third lithography steps are required for e-beam lithography devices. The double gate $MoTe_2$ transistor is fabricated with a bottom-up process. 30nm $Al_2O_3$ is deposited with atomic layer deposition (ALD) at 250°C on back-gated $MoTe_2$ transistors. Few-layer graphene flakes are then transferred as top gate covering the whole channel. The probing pad to the graphene flake is deposited afterward with an additional lithography process.

Two methods are used to fabricate the suspended $MoTe_2$ channel. The first method fabricates the trench first followed by transferring the flake on top, and then shadow masks are used for metalization of 5nm/40nm Ti/Au. The silicon substrate with 90nm oxide is first deposited with Al with the trench exposed through e-beam lithography. Then, the $SiO_2$ is etched in the RIE with 15sccm $CF_4$ gas flow for 3 minutes to completely remove the oxide. The $MoTe_2$ flakes are exfoliated using the PDMS stamp method and transferred over the trench. Copper grids are used as the shadow mask since the suspended structure is too delicate for regular lithography. The copper grid is carefully placed on top of the $MoTe_2$ flake under the optical microscope and fixed by tapes. Then, the stack is put in the deposition tool and the copper grid is simply removed after deposition to isolate the source and drain pads. This process simplifies the lithography process and protects the channel. The other method fabricates the back gate device first with Cr/Au 5nm/100nm as metal contacts to provide resistance against HF etchant. The substrate under the channel is then etched off in the HF solution. The substrate is carefully rinsed by flowing water and then IPA into the HF beaker. Drying with the $N_2$ gun will easily collapse the flake. A critical point dryer is used while the substrate is submerged in IPA in the whole process to preserve the suspended flake.

## 2.3 Characterization methods

Raman and photoluminescence spectroscopy are used to characterize individual flakes in the Renishaw micro-spectroscopy system. Figure 6 shows the Raman spectrum of $MoTe_2$ flakes for various layer thicknesses with laser excitation at 633nm. It is found that the intensity of out-of-plane mode $A_{1g}$ increases and the intensity of $B^1_{2g}$ peak increases as thickness decreases except for the $B^1_{2g}$ peak of the

monolayer. The energy of in-plane mode $E^1_{2g}$ experiences redshift from 1L to 4L. These three most prominent peaks confirm the $MoTe_2$ is in the 2H phase as compared with the previous report [42].

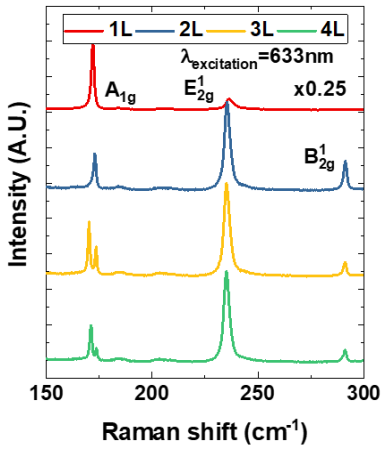


Figure 6. Raman spectrum for 1L-4L $MoTe_2$. The curves are shifted vertically for comparison with major peaks labeled.

The electrical characterization of devices is done with a Lakeshore probe station with a Keysight B1500A analyzer. The chamber of the probe station is vacuumed down to 1e-4 Torr, and all the measurements are conducted in the vacuum condition if unspecified. Keysight B1500A analyzer is used for electrical measurement. The photocurrent is measured in a home-built setup as shown in Figure 7. The setup is built from individual components, including laser source, monochromatic filter, mirrors, power meter, microscope, and probe station with a vacuum chamber. The laser is generated from the supercontinuum light source with a wavelength from 470nm to 1440nm and directed through the monochromatic filter with a fiber. A beam splitter is used to direct 50% of the power to the power meter, which allows runtime power monitoring. The laser is steered with multiple mirrors and passes through a tunable pinhole before entering the microscope. The microscope is equipped with an LED source as well as a camera with infrared sensibility. The laser spot is identified from the camera and the XYZ translation stage is used to move the sample according to the position of the laser spot. The probe station is built from MMR Technologies with four probing tips and a back gate, which are connected to the analyzer. A turbopump is connected to the probe station chamber, which can achieve a vacuum at 1e-5 Torr.

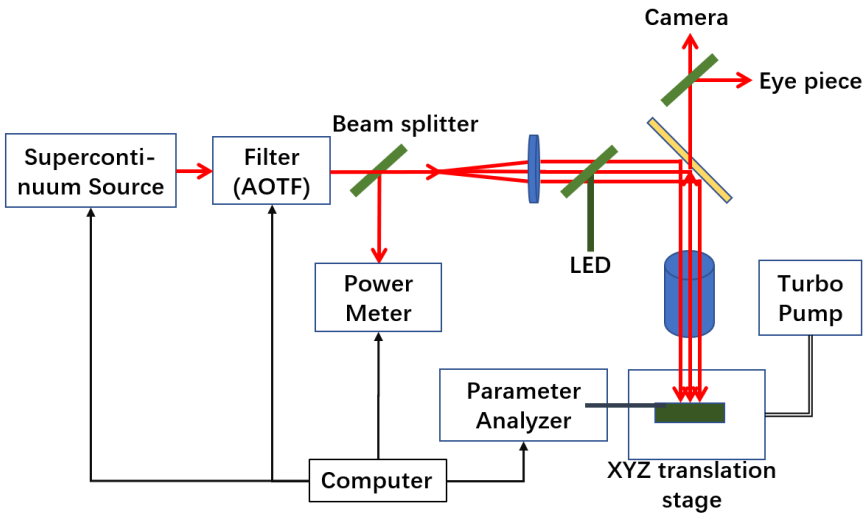


Figure 7. The setup of the home-build photocurrent measurement system. Aside from the parts shown, Labview program is designed and running in the computer which controls the laser source, filter, power meter, analyzer, and stage movement.

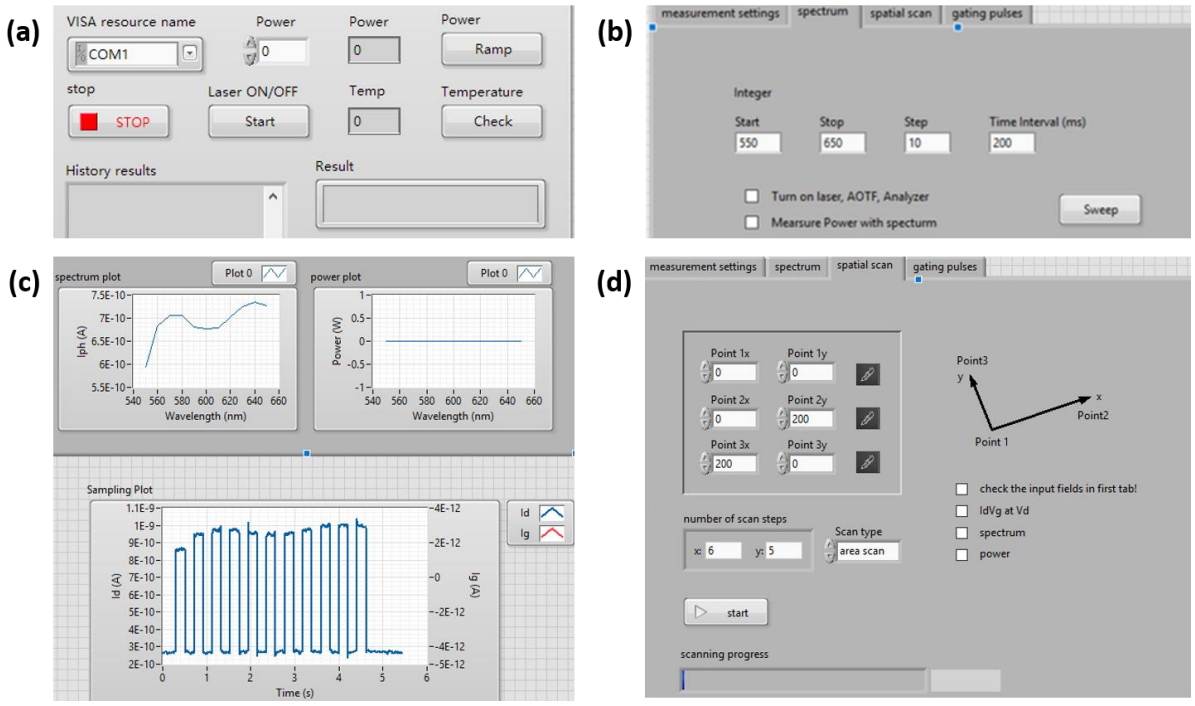


Figure 8. (a) Setting window for the laser source. (b) Setting window for the spectral photocurrent measurement. (c) Data display area for spectral photocurrent. (d) Setup window for the spatial photocurrent measurement.

Labview program is designed to control the individual components to automate various measurements. The control inputs for the laser source and monochromatic filter are shown in Figure 8(a). The filtered light is a laser with ~3nm linewidth. The measured power from the power meter will be displayed in the program. With the analyzer connected to the probe station, the photoresponse of the device can be measured in the program. Figure 8(b) shows the setting window for the spectral photocurrent measurement. Clicking the “sweep” button will execute the measurement. The laser will sweep for the range provided with both on/off cycles for each wavelength. The measured data is read from the analyzer and processed in the Labview program as shown in Figure 8(c). The bottom graph shows the original data read from the analyzer, and the “spectrum plot” graph in the top-left shows the photocurrent extracted for each wavelength by subtracting the off-cycle current from the on-cycle current. When the option to measure power is checked, the laser power at each wavelength will appear in the “power plot” graph in the top-right of Figure 8(c). Figure 8(d) shows the setting window for spatial photocurrent measurement. The scan area/line is defined by the first three/two sets of coordinates, and the steps define the spatial resolution in measurement. The measurement performed at each point is listed as checkboxes in the right. After clicking the “Start” button, the progress of scanning is shown in the bottom. The spatial scanning is achieved by two sets of picomotors attached to the XYZ translation stage. During the spatial measurement, the program transforms the scan area/line defined in the inputs into a list of points. The program drives the picomotors to the point on top of the list and starts the measurement requested. After the measurement is finished the stage is driven to the next point. Thus, spatial photocurrent can be measured pointwise until all the points are measured.

## 3. 2D transistors based on CVD grown $MoS_2$ and $WSe_2$

The monolayer $MoS_2$ and $WSe_2$ are synthesized using the CVD method in our research group and the processes and characterization results are reported in [43]. The typical optical images of $MoS_2$ and $WSe_2$ are shown in Figure 9. The monolayers are in good triangular shapes, and the Raman and photoluminescence spectra in [43] confirm that the synthesized flakes have good crystallinity. Here, the electrical performances of the synthesized flakes are examined by fabricating back-gated transistors. Different polarity behaviors are observed for $MoS_2$ and $WSe_2$. The contact resistance and channel resistance of $MoS_2$ transistors are determined using 4-point measurements. The field-effect mobilities are extracted and compared.

Two e-beam lithography steps are adopted for $MoS_2$ transistors to form alignment marks and source/drain contacts. 5nm Ti/ 40nm Au is used as the contact metals. The characterization results are summarized in Figure 10. Figure 10(a) shows the transfer curves of a transistor of CVD monolayer $MoS_2$. The optical image of the device is shown in the inset of Figure 10(a). The transistor is turned on when the gate voltage $V_g$ is above 40V, indicating an n-type behavior with a low Schottky barrier for electrons. The transfer curves of ± 1V drain biases are not overlapping due to asymmetric contacts. The hysteresis of the transfer curve is clockwise which can be attributed to the interfacial traps between $SiO_2$ and $MoS_2$. The field-effect mobility is extracted for the forward-sweeping branch at drain voltage $V_d$=-1V, shown in Figure 10(b). The peak mobility is 0.46$cm^2$/V·s, which is comparable to previous reports on CVD $MoS_2$ [44, 45]. However, the mobility is two orders of magnitude smaller than typical bulk value [46]. Figure 10(c) shows the output characteristics of the $MoS_2$ transistor. Strong gate modulation of the drain current is observed. The currents at 1V and -1V drain biases confirm the asymmetric conduction. The rectifying behavior indicates a finite Schottky barrier at the source/drain contacts. Figure 10(d) shows the characteristics of a Hall-bar device, whose optical image is shown in the inset. The distance between the two center sensing terminals is 4μm, and the length of the channel is 10μm. When 1V drain bias is applied, the channel resistance between two center terminals and the total resistance between source/drain terminals are measured using the 4-point measurement method. The contact resistance can be extracted from these measurements as:

$$2R_c = R_{total} - R_{channel}\frac{L_{SD}}{L_{center}} \quad (1)$$

where the $L_{sd}$ refers to the length between source and drain; $L_{center}$ is the distance between two center terminals. The total resistance and channel resistance decrease rapidly when the channel is turned on. At $V_g$=30V, the channel resistance $R_{channel}$ (24.8MΩ) is much higher than the contact resistance $R_c$(9.7MΩ). The peak field-effect mobility extracted from channel conductivity excluding contact resistance is 0.41cm$^2$/V·s. The high channel resistance and the similar mobility value extracted with and without considering contact resistance confirm that the drain current at large gate bias is limited by the channel conductivity, where high carrier scattering rate in the channel leads to low mobility.

40nm Pd is used as the contact metal for $WSe_2$ transistors to reduce the Schottky barrier for holes, and the standard three-step e-beam lithography is adopted. The added etching process ensures well-defined channel shapes for all devices. The characterization results are shown in Figure 11. Figure 11(a) shows the transfer curve of a $WSe_2$ transistor at $V_d$=0.2V. The transistor is at on state when the gate is biased at a negative voltage, indicating a p-type behavior, which is opposite to the $MoS_2$ case. This p-type transport is facilitated by the high work function of Pd. The hysteresis for the $WSe_2$ transistor is counter-clockwise due to interfacial traps. The mobility extracted from the backward sweep peaks at 20cm$^2$/V·s, shown in Figure 11(b). The mobility of monolayer $WSe_2$ is higher than monolayer $MoS_2$. However, the $WSe_2$ devices show a strong device-to-device variation. Figure 11(c) shows the statistics on 20 $WSe_2$ transistors fabrication with the same process condition. The majority of the devices show peak mobilities in the range of 0~6cm$^2$/V·s. The non-uniformity in mobility values suggests that further improvements in the synthesis and fabrication process can achieve high mobility $WSe_2$ transistors at the monolayer limit by reducing the defect density and grain boundaries.

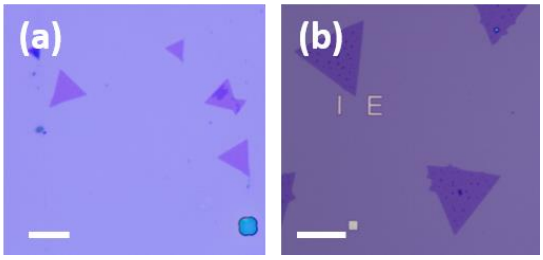


Figure 9. Typical optical image of $MoS_2$(a) and $WSe_2$(b) on Si/280nm $SiO_2$. The scale bars are 20μm and 50μm respectively.

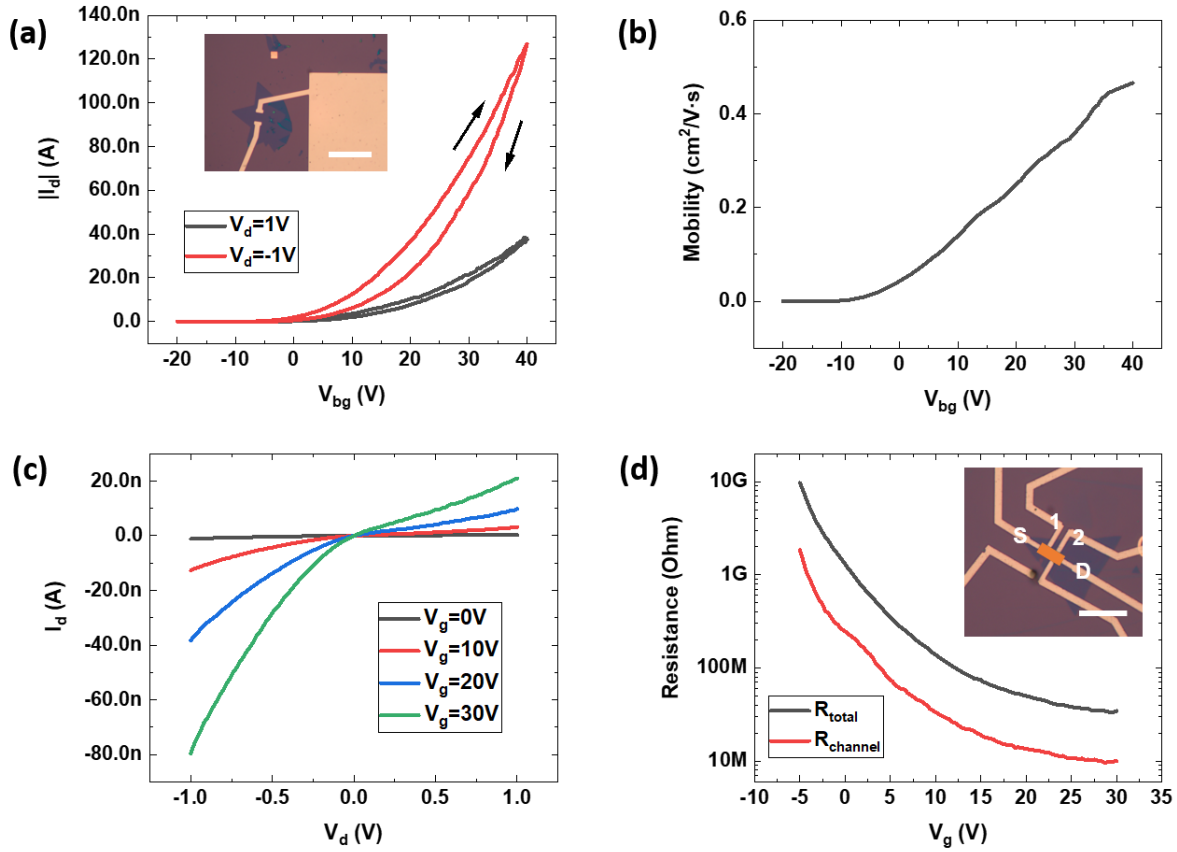


Figure 10. Scale bar: 10µm. (a) Transfer curves of the $MoS_2$ transistor shown in the inset image at $V_d$=1V and -1V. (b) Mobility extracted from the forward-sweeping $I_d$-$V_g$ at $V_d$=1V. (c) $I_d$-$V_d$ characteristics of the device shown in (a). (d) Channel resistance and total resistance measured from the Hall-bar device shown in the inset.

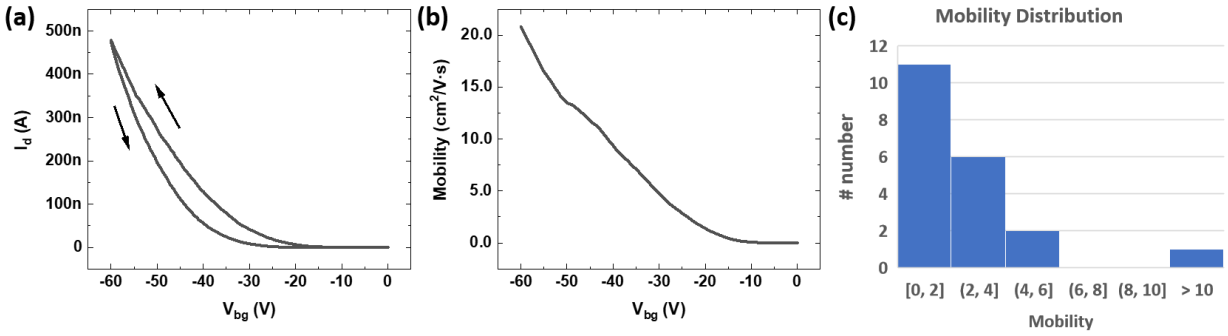


Figure 11. (a) Transfer curve of a $WSe_2$ transistor at $V_d$=0.2V. (b) Extracted mobility from the backward sweep is shown. (c) Histogram of peak field-effect mobilities extracted from 20 transistors.

# 4. 2D transistors based on exfoliated $MoTe_2$

## 4.1 Back gate transistors

Various electrical parameters are extracted for $MoTe_2$ from back gate transistors. $MoTe_2$ flakes are exfoliated through the PDMS stamp method and transferred to Si substrate with 280nm $SiO_2$. The mobilities and Schottky barrier height for electrons are extracted for back-gated $MoTe_2$ transistors fabricated using photolithography with Cr/Au 5nm/40nm as metal contacts. Ambipolar $MoTe_2$ transistors are fabricated using e-beam lithography with 40nm Pd as the metal contact, where the bandgap is extracted through spectral photocurrent and temperature-dependent minimum conductance.

Figure 12(a) shows the temperature-dependent transfer curves of a fabricated $MoTe_2$ transistor with $V_d$=0.2V. The channel thickness is estimated from optical contrast as ~10nm. The device shows a strong electron branch along with a weak hole branch. The transfer characteristics can be categorized into three regions based on the barrier height extracted in Figure 12(b). Between $V_g$=-60V and $V_g$=3V is the p branch of the transfer curve. For Vg between 3V and 18V, the transfer curves have a steep slope which corresponds to the thermionic tunneling of carriers. The ideal subthreshold swing (SS) in this region equals 2.3kT, where k is the Boltzmann constant and T is the temperature. The SS measured at different temperatures are 0.990V/dec at 300K, 0.752V/dec at 280K, and 0.571V/dec at 260K. The large SS is due to the fact that the interface trap capacitance is comparable with the dielectric capacitance. As temperature rises, the active interface trap density also increases. The Schottky barrier for electrons at the flat band is determined to be 0.20eV at $V_d$=0.2V and $V_g$=18V, which is consistent with strong n-type behavior in transfer curves. For $V_g$ larger than 18V, thermo-assisted tunneling starts to contribute to the current as characterized by reduced $I_d$~$V_g$ slope and weak temperature dependence. The barrier height decreases monotonically as gate bias increases. A barrier height as low as 0.04eV is observed at $V_g$=60V due to increased tunneling probability as the injection barrier is thinned. Figure 12(c) shows the $I_d$-$V_d$ characteristics of the same device at $V_g$=60V when the transistor is turned on. The output curves clearly show drain current saturation due to channel pinch-off. The symmetric behavior for positive and negative drain biases indicates an ohmic contact is achieved at large gate bias. Figure 12(d) shows the temperature-dependent electron mobility extracted from (a) at a constant overdrive voltage. The room temperature mobility is 8 $cm^2/V{\cdot}s$. However, the mobility degrades at low temperatures due to strong

Coulomb scattering. The fabrication includes exposure to ion-containing developers, which is a source of the charged impurities.

Aside from the Schottky barrier, the bandgap is extracted for bulk $MoTe_2$. An image of $MoTe_2$ Hall-bar device fabricated with e-beam lithography is shown in Figure 13(a). A high-work-function metal Pd allows achieving of ambipolar behavior. The spectral photocurrent of the device is measured and the bandgap is extracted in Figure 13(b). The laser is shined in the middle of the device and the source and drain metal pads are used as sensing terminals. By assuming an indirect transition for the 3-dimensional density of state with a parabolic valley, the absorption of semiconductor, $\alpha$, near the band edge can be formulated as:

$$(\alpha h\nu)^2 = A\left(h\nu - E_g\right) \tag{2}$$

where $h$ is the Planck constant, and $h\nu$ refers to the energy of incident light; $A$ is the coefficient; $E_g$ is the bandgap. Since the photocurrent is proportional to the absorption, the bandgap of $MoTe_2$ can be extracted by linear fitting in the plot of $(I_{ph}h\nu)^2$ near the band edge, where $I_{ph}$ is the spectral photocurrent. The measured 1.013eV bandgap is close to previous reports [47]. The bandgap of the flake at the channel is also extracted from the temperature-dependent minimum conductance. As is shown in Figure 13(c), transfer curves measured at various temperatures are plotted. The conductances are measured through the 4-point measurements. The dependence of minimum conductance on temperature is given as:

$$\frac{\sigma}{\sqrt{\mu_n \mu_p}} = 2n_i \propto \exp\left(\frac{E_g}{2kT}\right) \tag{3}$$

where $\mu_n$ and $\mu_p$ are the mobility for electrons and holes; $n_i$ is the temperature-dependent intrinsic carrier density. For the temperature range of interest, the temperature dependence of mobility is neglected. Therefore, the minimum conductivity simply increases exponentially as 1/T decreases. Figure 13(d) plots the minimum conductance in the log scale at each temperature. The bandgap extracted from linear fitting gives $E_g$=0.946eV. The extracted bandgap from these two methods matches well with each other.

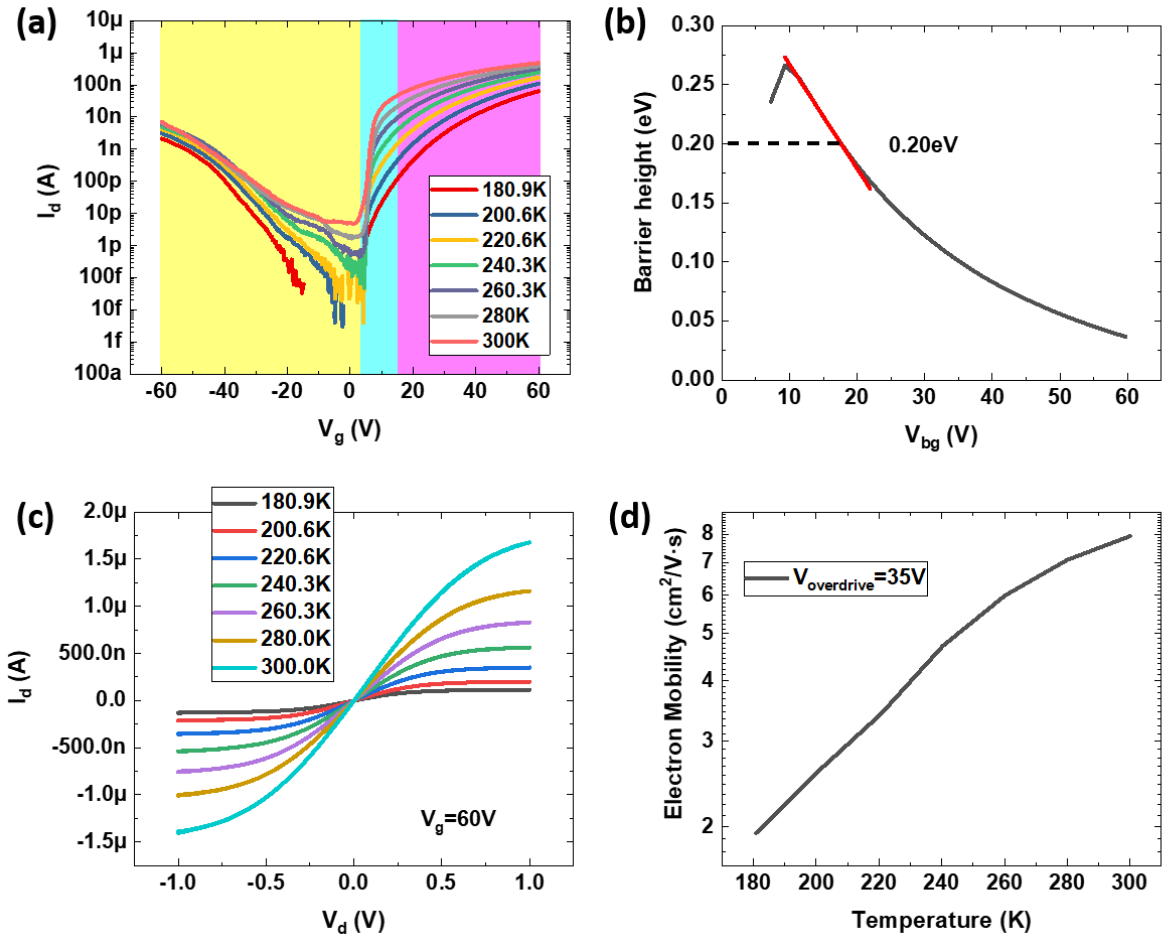


Figure 12. Variable temperature characterization of a back-gated MoTe2 transistor from 180.9K to 300K. (a) Transfer characteristics at various temperatures. (b) Extracted Schottky barrier height for electrons at different gate biases. (c) Output characteristics at different temperatures. (d) Electron mobility as a function of temperature.

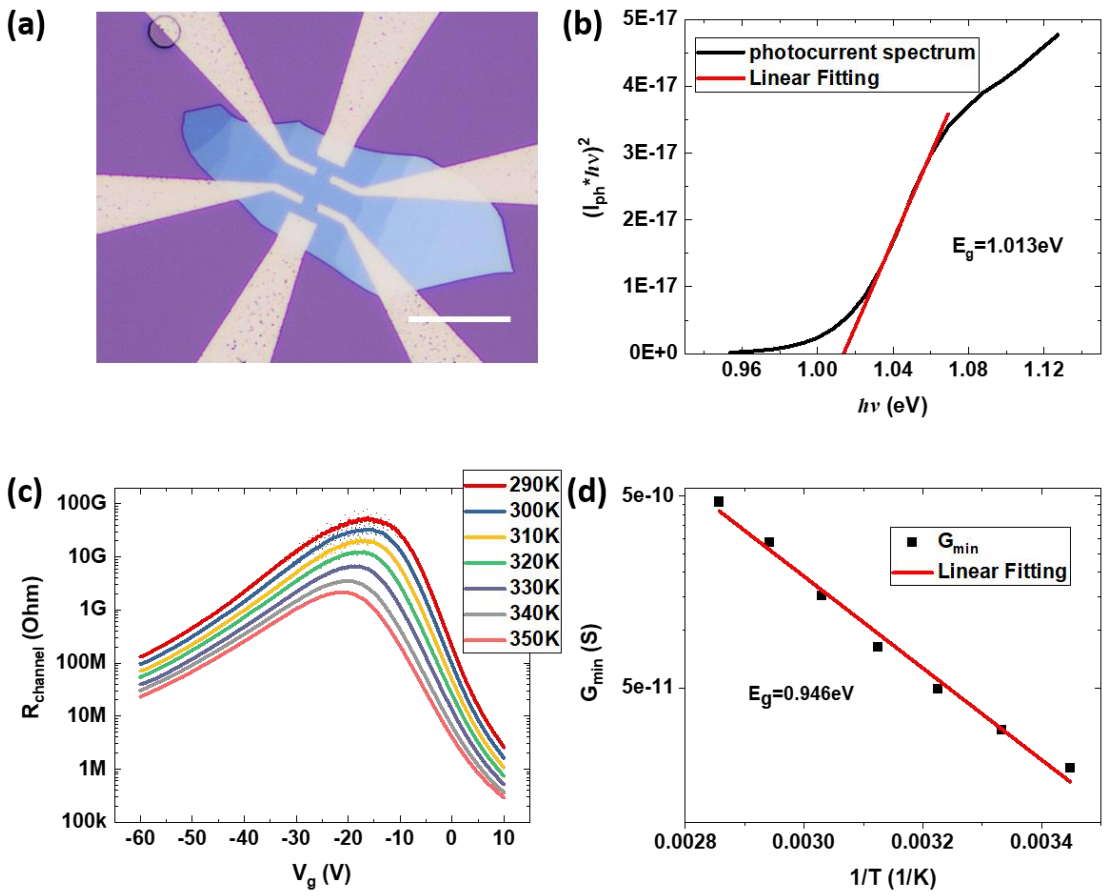


Figure 13. Bandgap extraction for $MoTe_2$. (a) Optical image of a $MoTe_2$ Hall-bar device fabricated with e-beam lithography and Pd as the contact metal. The scale bar is 20μm. (b) Normalized spectral photocurrent near the band edge with the linear fitting for bandgap extraction. (c) Temperature-dependent channel resistance extracted from the $MoTe_2$ device from 290K to 350K. (d) Minimum conductances for each curve are plotted against 1/T in the log scale, where the bandgap is extracted from the slope.

## 4.2 Suspended transistors

Suspended transistors are ideal for studying the intrinsic mobility of channels without the dielectric [22]. $MoTe_2$ suspended transistors are fabricated through the transfer-over-trench method and the substrate-etching method. The first method allows direct comparison of suspended and supported regions for thin flakes, where Raman and AFM characterizations are performed. The substrate-etching method suspends the whole channel area, where intrinsic electrical performance can be assessed. The temperature-dependent channel and contact resistance are compared and the temperature dependence of mobility is extracted and compared with that of supported devices.

Figure 14 shows the characterization results of suspended transistors fabricated with the transfer-over-trench method. A $MoTe_2$ flake on the prefabricated trench in the Si substrate with 90nm $SiO_2$ is shown in Figure 14(a). The flake is bent downward in the suspended region according to AFM mapping shown in Figure 14(b). The measured transfer curve and the optical image of a suspended device at ambient conditions are shown in Figure 14(c). The mobility of the channel is nearly unchanged here since the supported region on $SiO_2$ is much longer than the suspended region. Therefore, the transfer curve here resembles the transfer curve of supported devices, where the interface traps introduce large hysteresis, and surface scattering greatly degrades the mobility. Suspended flakes show dramatic differences in Raman spectroscopy compared with supported flakes as shown in Figure 11(d). The out-of-plane $A_{1g}$ mode and $B^1_{2g}$ mode are characteristic for few-layer $MoTe_2$ flakes [48]. The suspended flake shows enhanced absorption in out-of-plane $A_{1g}$ mode and reduced absorption in in-plane $E^1_{2g}$ mode, while the $B^1_{2g}$ mode is completely suppressed. These changes are presumably owing to the additional strain introduced in suspended flakes and the absence of surrounding dielectrics.

Figure 15 shows the intrinsic electrical characteristics of suspended $MoTe_2$ transistors revealed by completely suspending the channel region. The SEM image is shown in comparison with a supported device in Figure 16. Figure 15(a) depicts the transfer curves at different temperatures at $V_d$=2V. The device shows n-type behavior at all temperatures. The threshold voltage drifts as temperature increases. The measured hysteresis is negligible which confirms that the suspended channel is free of interface trap. Figure 15(b) shows the $I_d$-$V_d$ characteristics at $V_g$=20V for various temperatures. The $I_d$-$V_d$ shows ohmic behavior with linear characteristics at high temperatures. Figure 15(c) and (d) show the channel resistance and contact resistance extracted from the 4-point measurement. The channel resistance is substantially higher at low temperatures due to strong scattering from charged impurities. These two resistances manifest significant differences in the subthreshold region at 300K. The slope in

the subthreshold region of channel resistance is larger compared with contact resistance. The inconsistency between channel and contact resistance is due to the different gate dielectrics in the channel and contact region.

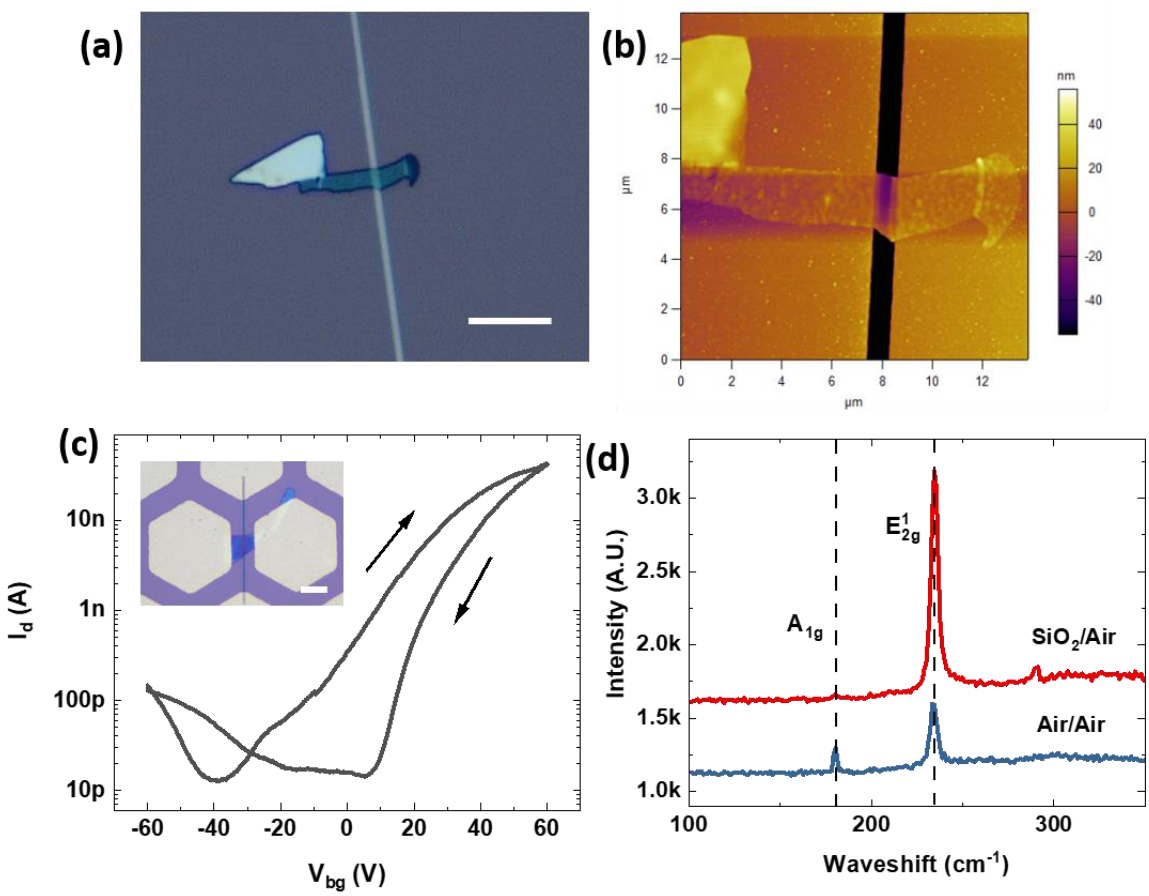


Figure 14. (a) Optical image showing a $MoTe_2$ flake is suspended over a trench. (b) AFM image of the flake shown in (a) reveals the bending in the suspended region. (c) $I_d$-$V_g$ characteristics of a suspended channel transistor that shows ambipolar behavior. (d) Comparison of Raman spectra for suspended and supported flakes. All scale bars: 10μm.

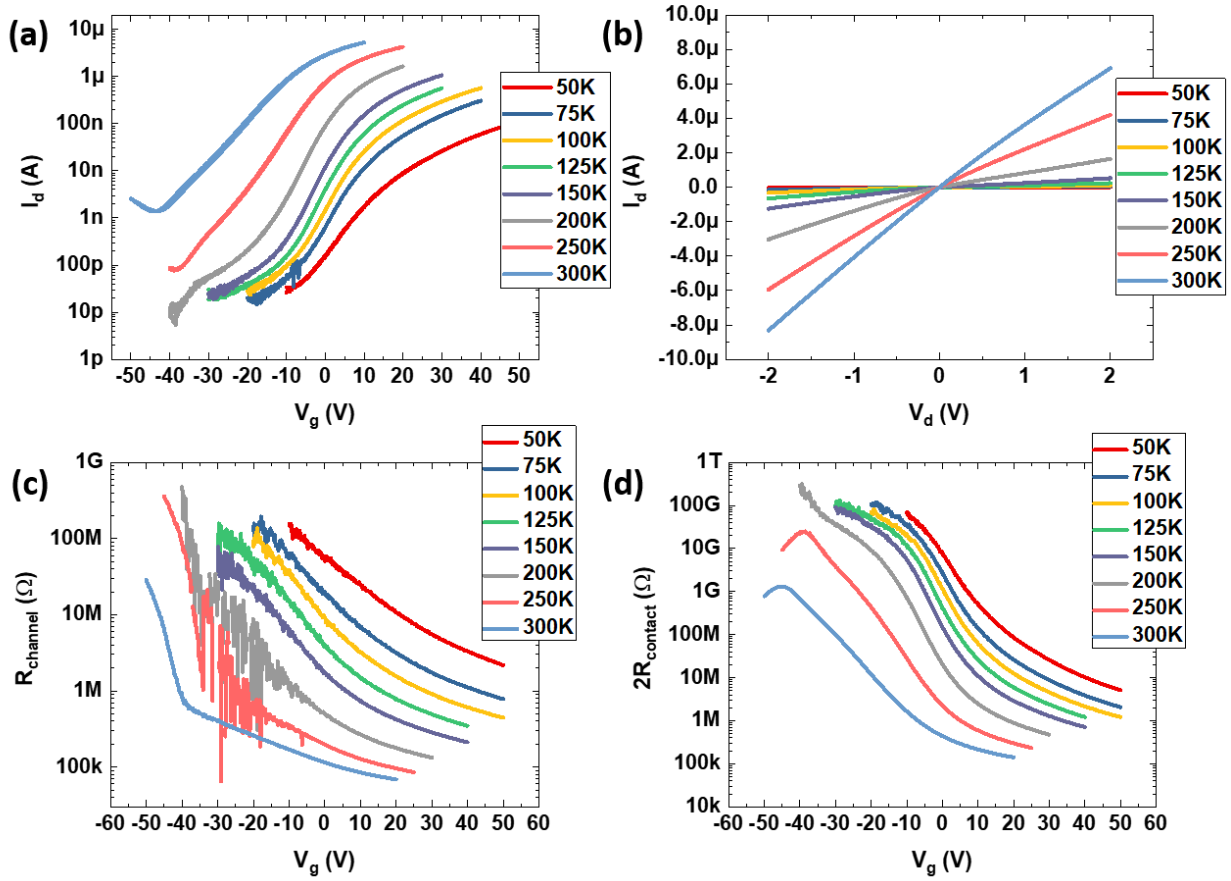


Figure 15. Temperature-dependent behavior of suspended transistors from 50K to 300K. (a) $I_d$-$V_g$ characteristics at different temperatures with $V_d$=2V. (b) Temperature-dependent output characteristics at $V_g$=20V. (c) Gate dependence of channel resistance at various temperatures. (d) Gate-dependent contact resistance at various temperatures.

Figure 16 compares the temperature-dependences of mobility between suspended devices and supported devices. Both devices are fabricated with the same processes, except the dielectric was etched for the suspended device after fabrication. Figure 16(a) and (b) show the schematic and optical image respectively for the regular $MoTe_2$ device used for comparison, where the $SiO_2$ layer is intact and serves as the dielectric for Si back gate. Figure 16(c) and (d) show the schematic and SEM image respectively for the suspended $MoTe_2$ device, where the air gap under the channel serves as the dielectric. Both channels are thick and show strong n-type behaviors that resemble the bulk material. The temperature-dependent mobilities for both devices are extracted at the same overdrive voltage and presented in Figure 16(e). The mobility of the supported device decreases at 275K due to phonon scattering. The high-temperature mobility of the suspended channel reaching 108 $cm^2/V{\cdot}s$ is much

higher than that of the supported channel at 39 $cm^2/V{\cdot}s$ due to reduced phonon scattering. However, the mobility of the suspended channel falls in the low-temperature region. This is presumably due to the absence of dielectric screening of charged impurities [49]. Additionally, extra charged impurities are possibly introduced during the dielectric etching.

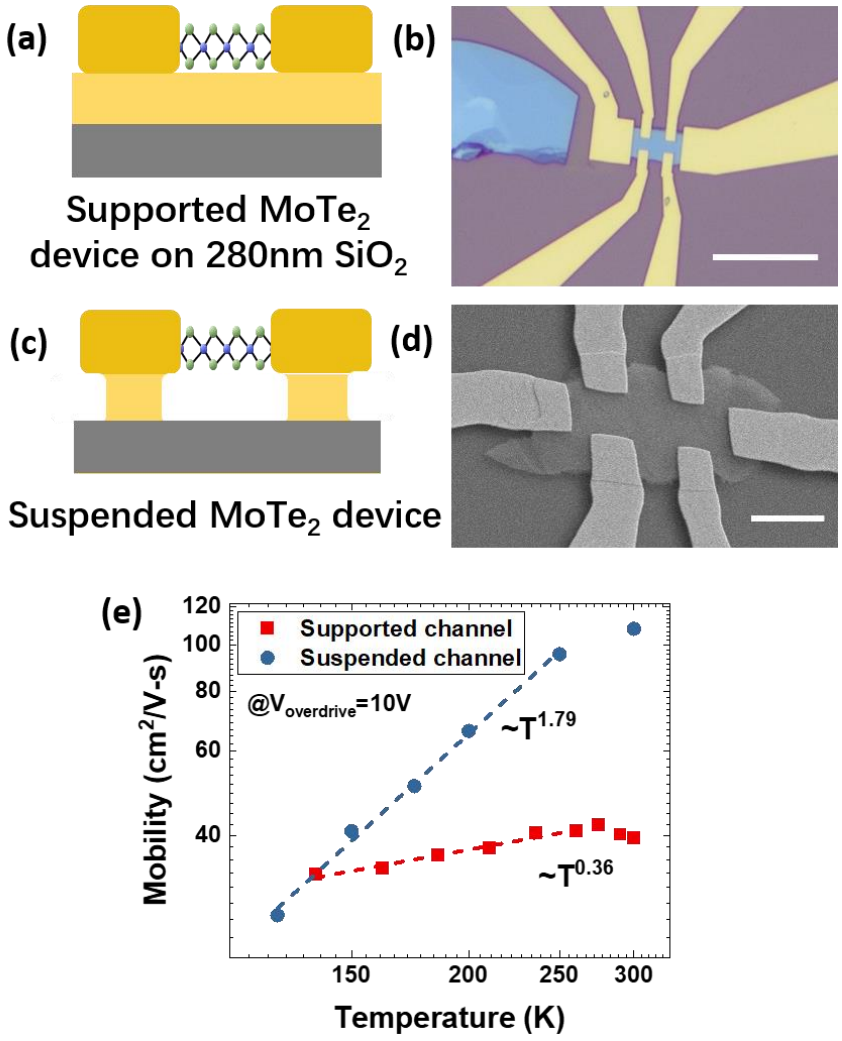


Figure 16. (a) (b) Schematic and the optical image of a supported device. The scale bar is 20μm. (c) (d) Schematic and SEM image of a suspended device. The scale bar is 5μm. (e) Temperature-dependent mobility extracted from the supported device and suspended device at a fixed overdrive voltage.

## 4.3 Double gate transistors

Double gate transistors based on bilayer $MoTe_2$ are fabricated by adding top dielectric and top gate on back gate devices. The bias on the additional gate not only dopes the channel electrostatically but establishes a vertical electric field. Both photolithography and e-beam lithography devices are fabricated. The electrostatic doping from the additional gate is investigated for devices fabricated with different methods. The effect of the vertical electric field is discussed. The photocurrent response of the double gate transistor is also analyzed.

Figure 17 shows the transfer curves for various combinations of gate voltages for a device fabricated with photolithography. Figure 17(a) shows the optical image of the fabricated device before the top gate deposition. The channel is bilayer $MoTe_2$ as determined from the optical contrast. The semi-transparent few-layer graphene allows light to be absorbed by the channel and induce photocurrent. Figure 17(b) shows the back gate sweeps at fixed top-gate voltages. The transfer curves show ambipolar behavior in contrast to the n-type behavior for bulk flakes. As the top gate voltage increases from -4V to 4V, the charge neutrality point shifts by -2.7V. Considering the bottom gate dielectric is 90nm $SiO_2$ and the top dielectric is 30nm ALD $Al_2O_3$, the charge introduced by 8V in the top gate is equivalent to 55V in the back gate, which is much larger than the neutrality voltage shift of 2.7V observed in the experiment. This indicates that the Fermi level in the $MoTe_2$ channel is not effectively tuned by the top gate. A different behavior was observed for the top gate sweep shown in Figure 17(c). The polarity of transfer curve switches from n-type at $V_{bg}$=-8V, to p-type at $V_{bg}$=8V, indicating the Fermi level of $MoTe_2$ at contacts is tuned effectively. This discrepancy in the top and back gate sweeps can be explained as follows. The injection of current occurs near the contact which is only accessible through the back gate. The Schottky barrier at the contact controls the polarity of transfer curves. With sufficient doping from the back gate, the metal-$MoTe_2$ Schottky barrier can be tuned in a wide range, allowing switching between n-type and p-type. Moreover, as for the top gate bias, the residue layer of photoresist on the top channel surface may prohibit the depletion of the whole channel, as indicated by the low on-off ratio in Figure 17(c).

In addition to the electrostatic doping, double gate bias also establishes a vertical field across the channel. Figure 13(c) shows that the minimum conduction is directly related to the mobility and bandgap of the channel materials. The behavior of minimum conductance under a vertical electric field is examined here. The maximum vertical displacement field applied is 1.44V/nm. The device in Figure 18(a) is fabricated through e-beam lithography, where a low-residue surface is achieved. The minimum conductances in back gate sweeps shown in Figure 18(b) remain constant at different top gate voltages.

The maximum channel resistances extracted from the 4-point measurements in Figure 18(c) are also constant. These behaviors indicate the doping level in the contact region is controlled by both top and back gates. The combination of top and back gate voltages at minimum conductance points leads to identical doping concentration under the contact and in the channel, and therefore to identical minimum conductance. Here, 2V change in the top gate results in a 35V shift in the back-gate transfer curve, which is more effective compared with Figure 17(b).

The photocurrent of the $MoTe_2$ transistor under double gate biases is also investigated. Figure 19(a) shows the top gate sweeping characteristics of the device under test shown in the inset image. The device shows similar polarity switching behavior as in Figure 17. The photocurrent mapping is plotted for various top and back gate voltages in Figure 19(b). The incident photon energy is set at 1eV which corresponds to the exciton energy of bilayer $MoTe_2$. The highest photocurrent occurs when both top and back gates are biased at the positive limits, while the photocurrent is smallest when the channel is close to charge neutrality, which is near the center of the mapping. This suggests that the photocurrent is generated from the Schottky barrier, where a large band bending by large gate biases leads to large photocurrent.

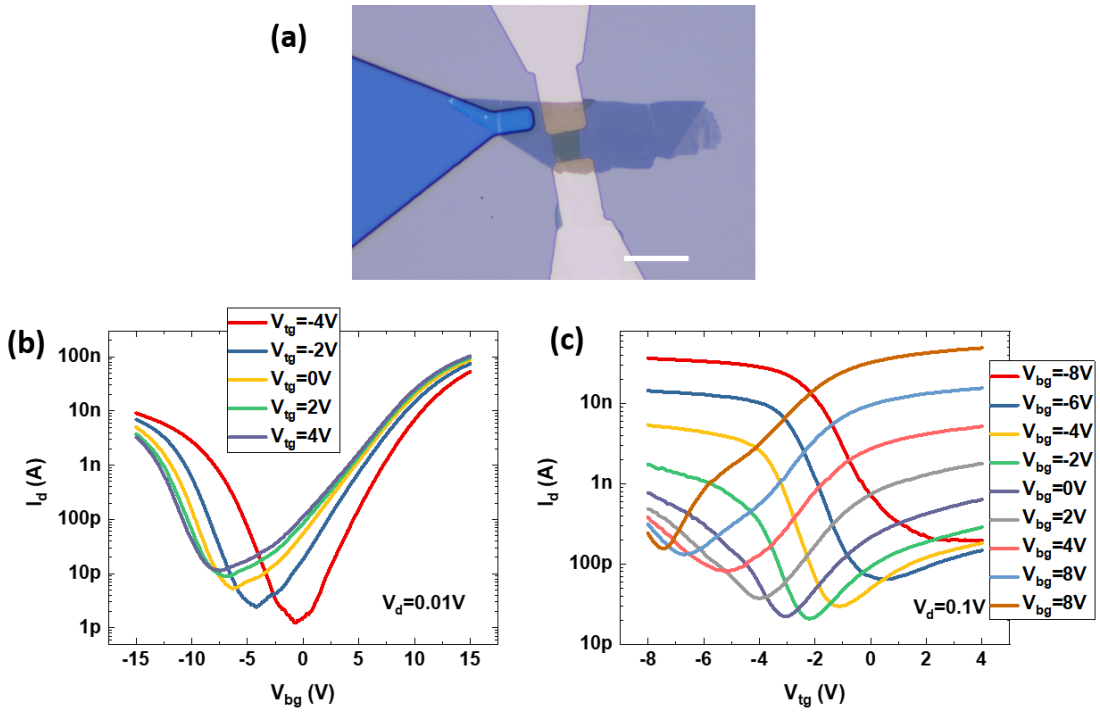


Figure 17. Top and back gate sweeps for double gate $MoTe_2$ transistor. (a) Optical image of a device before the top gate deposition. The scale bar is 20μm. (b) Transfer curves from the back-gate sweep at various top gate voltages. (c) Transfer curves from the top-gate sweep at various back gate voltages.

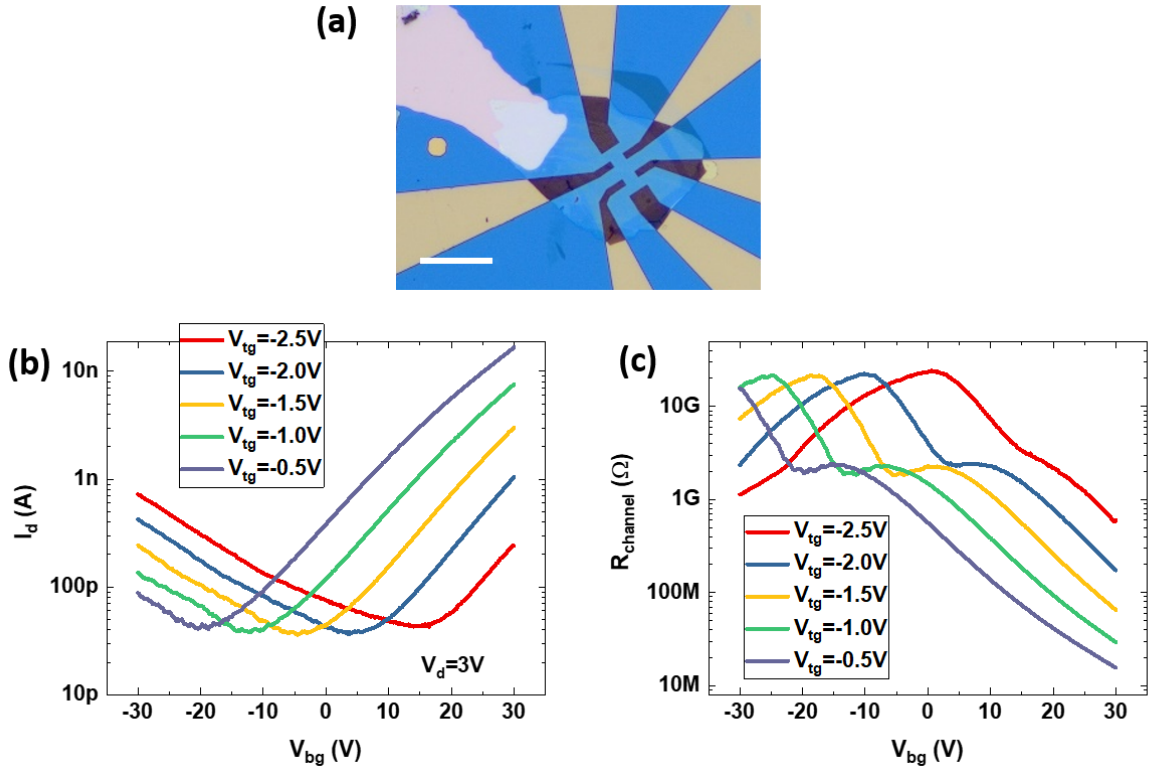


Figure 18. (a) Optical image of double gate bilayer $MoTe_2$ device fabricated with e-beam lithography. The scale bar is 20μm. (b) Back-gate $I_d$-$V_g$ characteristics at different top gate voltages. (c) Gate-dependent channel resistances extracted from 4-point measurement with the same condition in (b).

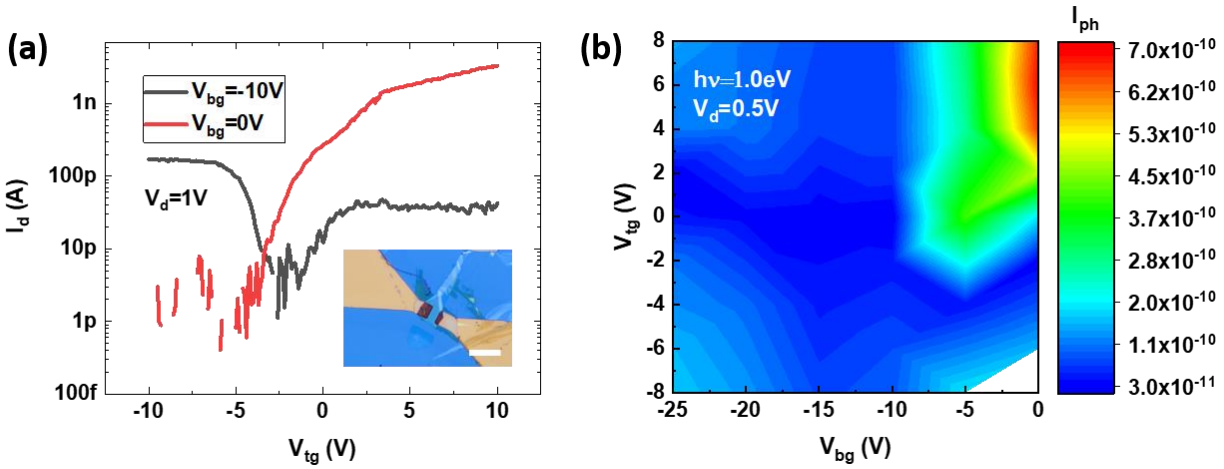


Figure 19. (a) Polarity switching induced by back-gate biasing for the shown double gate bilayer $MoTe_2$ device. The optical image of the device before the top gate deposition is shown in the inset image. The scale bar is 20μm. (b) The photocurrent mapping for different combinations of back-gate and top-gate voltages.

# 5. Conclusion

We developed the fabrication process for electronic and optoelectronic devices based on various TMDs and established automated photocurrent measurements using Labview. Electrical transport of CVD synthesized $MoS_2$ and $WSe_2$ is systematically studied. In addition, three types of devices are fabricated based on exfoliated few-layer $MoTe_2$. Fast identification of flake thicknesses is achieved by the contrast-thickness correlation and Raman spectra. Electrical parameters such as mobility, Schottky barrier, and bandgap are extracted. The bandgap extracted from photocurrent spectrum and temperature-dependent intrinsic conductance are 1.013eV and 0.946eV respectively. The 10nm $MoTe_2$ channel with a mobility of 8 $cm^2/V{\cdot}s$ shows Schottky barrier limited behavior with the barrier height extracted as 0.2eV from temperature-dependent measurements. The room temperature mobility is further improved in suspended devices, where high room temperature mobility at 108 $cm^2/V{\cdot}s$ is achieved due to reduced phonon scattering. However, the absence of dielectric screening leads to low low-temperature mobilities. Moreover, the enhanced out-of-plane $A_{1g}$ mode is identified as a signature for suspended flakes. The effects of electrostatic doping and vertical electric field induced by the top gate on the current transport are investigated in double-gated devices. By controlling the electrostatic doping in the contact area, the polarity of the double gate device can be switched between n and p-type. The intrinsic conductance under a vertical electric field of 1.44V/nm is investigated, where constant minimum conductance is observed. In addition, the photovoltaic effect at the contact is identified as the photocurrent mechanism in the double gate transistor.

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